Refine Search

Search Results -

Terms	Documents
(interrupt near3 register) same (disabl$3 near3 register) same (mask$3 near3 register)	77

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	(interrupt near3 register) same (disabl$3 near3 register) same (mask$3 near3 register)	77	L2
L1	(interrupt near3 register) same ((disabl$3 or mask$3) near3 register)	1149	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	(interrupt near3 register) same (disabl$3 near3 register) same (mask$3 near3 register)	77	L2
L1	(interrupt near3 register) same ((disabl$3 or mask$3) near3 register)	1149	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and "interrupt mask register"	2

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	l1 and "interrupt mask register"	2	L3
L2	l1 same "interrupt mask register"	0	L2
L1	(mask adj1 value) adj3 stor$3 adj3 register	35	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and (mask$3 same (value or level)).ab.	15

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L3	L1 and (mask$3 same (value or level)).ab.	15	L3
L2	L1 and mask$3.ab.	45	L2
L1	710/262.ccls.	214	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and interrupt.ab.	46

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	l1 and interrupt.ab.	46	L3
L2	L1.ab.	4	L2
L1	(interrupt near3 register) same (mask adj2 register) same value	159	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1.ab.	4

Database:

- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	L1.ab.	4	L2
L1	(interrupt near3 register) same (mask adj2 register) same value	159	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1.ab.	4

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	L1.ab.	4	L2
L1	(interrupt near3 register) same (mask adj2 register) same value	159	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(344/418 |370/908 |710/260 |710/261 |710/262 |710/263 |710/264 |710/265 |710/266 |710/313 |710/48 |710/49 |711/100 |340/825 |712/32 |712/36 |712/233 |712/244 |714/34).ccls.	3992

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L1	710/260-266,313,48,49;714/34;712/32,36,233,244;711/100;344/418;340/825;370/908.ccls.	3992	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L2	27

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

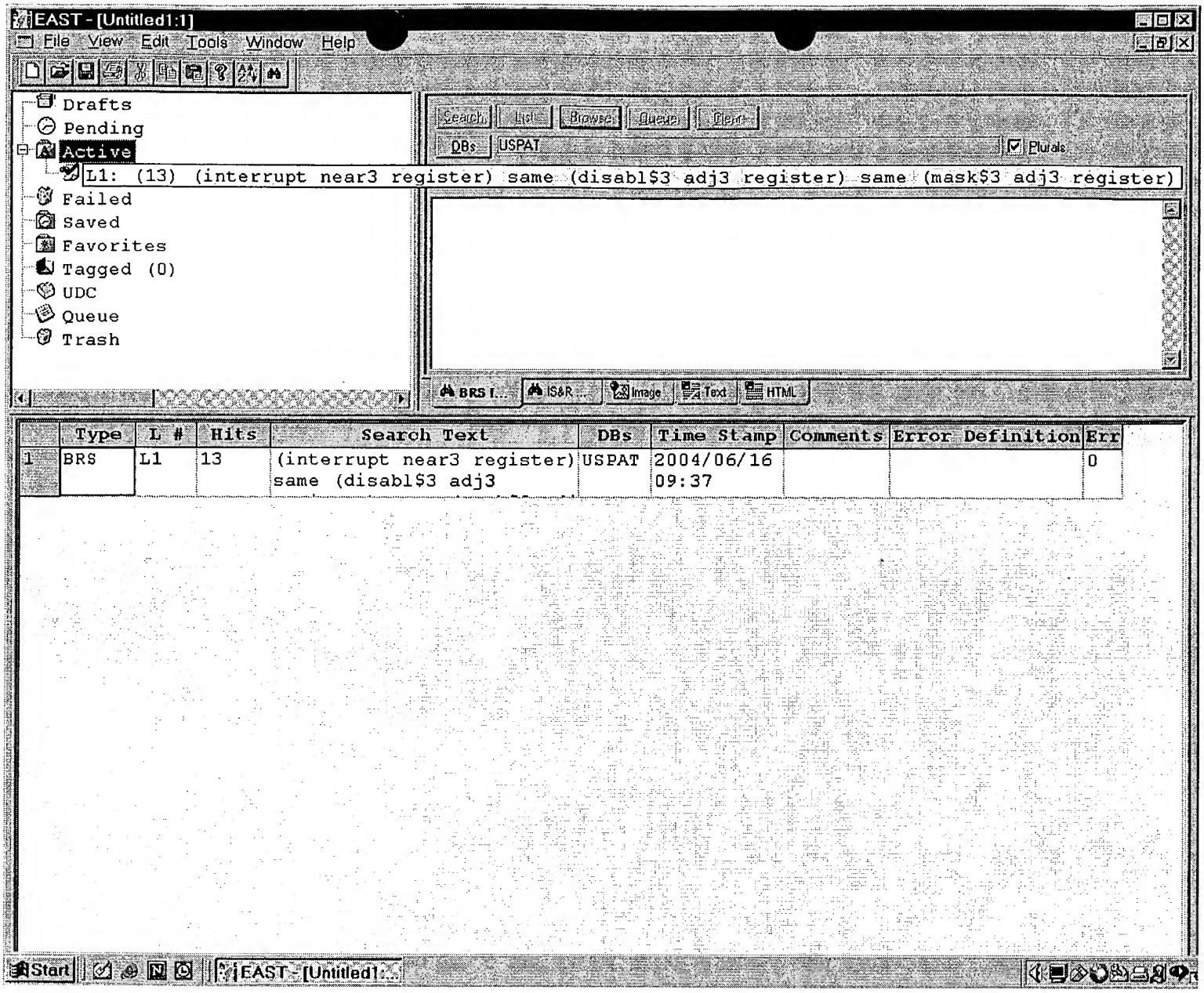
Search History

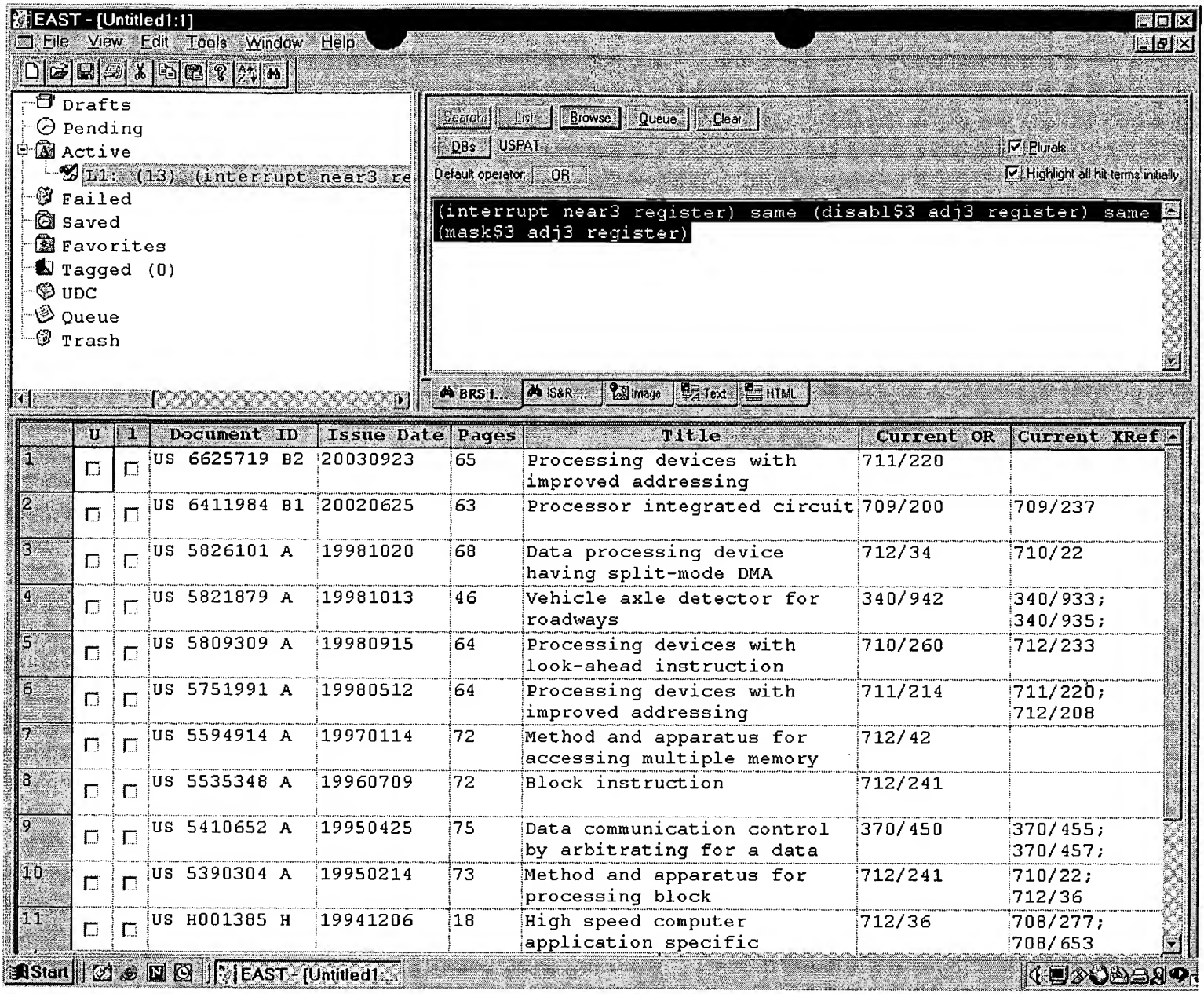
DATE: Wednesday, June 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L3	l1 and l2	27	L3
L2	(interrupt near3 register) same (disabl$3 near3 register) same (mask$3 near3 register)	77	L2
L1	710/260-266,313,48,49;714/34;712/32,36,233,244;711/100;344/418;340/825;370/908.ccls.	3992	L1

END OF SEARCH HISTORY

h e b b cg b e e ch


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (13) (interrupt near3 register) same (disabl$3 adj3 register) same (mask$3 adj3 register)
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search List Browse Queue Client
DBs USPAT
Plurals
BRS I... IS&R... Image Text HTML
Type L # Hits Search Text DBs Time Stamp Comments Error Definition Err
1 BRS L1 13 (interrupt near3 register) same (disabl$3 adj3 USPAT 2004/06/16 09:37 0
Start
EAST - [Untitled1:...



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6625719 B2	20030923	65	Processing devices with improved addressing	711/220	
2	☐	☐	US 6411984 B1	20020625	63	Processor integrated circuit	709/200	709/237
3	☐	☐	US 5826101 A	19981020	68	Data processing device having split-mode DMA	712/34	710/22
4	☐	☐	US 5821879 A	19981013	46	Vehicle axle detector for roadways	340/942	340/933; 340/935;
5	☐	☐	US 5809309 A	19980915	64	Processing devices with look-ahead instruction	710/260	712/233
6	☐	☐	US 5751991 A	19980512	64	Processing devices with improved addressing	711/214	711/220; 712/208
7	☐	☐	US 5594914 A	19970114	72	Method and apparatus for accessing multiple memory	712/42	
8	☐	☐	US 5535348 A	19960709	72	Block instruction	712/241	
9	☐	☐	US 5410652 A	19950425	75	Data communication control by arbitrating for a data	370/450	370/455; 370/457;
10	☐	☐	US 5390304 A	19950214	73	Method and apparatus for processing block	712/241	710/22; 712/36
11	☐	☐	US H001385 H	19941206	18	High speed computer application specific	712/36	708/277; 708/653

Your search matched **6** of **1045422** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

interrupt and register and bus Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **High speed data bus macro instruction set architecture**
Prohofsky, T.;
Aerospace and Electronics Conference, 1991. NAECON 1991., Proceedings of IEEE 1991 National , 20-24 May 1991
Pages:192 - 196 vol.1

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

---

2 **VICbus: VME inter-crate bus-a versatile cable bus**
Parkman, C.F.;
Nuclear Science, IEEE Transactions on , Volume: 39 , Issue: 2 , April 1992
Pages:77 - 84

[Abstract] [PDF Full-Text (756 KB)] **IEEE JNL**

---

3 **A reusable microcontroller core's design**
Janiszewki, I.; Baraniecki, R.; Siekierska, K.;
Fall VIUF Workshop, 1999. , 4-6 Oct. 1999
Pages:14 - 19

[Abstract] [PDF Full-Text (636 KB)] **IEEE CNF**

---

4 **An ASIC RISC-based I/O processor for computer applications**
Cates, R.L.; Farrell, J.J., III;
Euro ASIC '90 , 29 May-1 June 1990
Pages:50 - 55

[Abstract] [PDF Full-Text (484 KB)] **IEEE CNF**

---

5 **Rapid migration to VLSI**

Lowinski, W.B.; Kirwan, R.; Perry, A.; Yu, T.;
Aerospace and Electronic Systems Magazine, IEEE , Volume: 7 , Issue: 9 , Se
1992
Pages:21 - 23

[Abstract] [PDF Full-Text (216 KB)] **IEEE JNL**

---

6 **Design of optical-electrical encoder pulse counting card based on P(**
Qian Dong; Hanying Me;
Intelligent Control and Automation, 2002. Proceedings of the 4th World Cong
on , Volume: 3 , 10-14 June 2002
Pages:2194 - 2197 vol.3

[Abstract] [PDF Full-Text (481 KB)] **IEEE CNF**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

h eee e eee g e ch e ch e e c e e e c e

Your search matched **0** of **1045422** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

interrupt and register<and>disabl* and mask* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

Results:
No documents matched your query.

h eee e eee g e ch e ch e e e eg e c e

Rapid migration to VLSI

Lowinski, W.B. Kirwan, R. Perry, A. Yu, T.

This paper appears in: **Aerospace and Electronic Systems Magazine, IEEE**

Publication Date: Sept. 1992
On page(s): 21 - 23
Volume: 7 , Issue: 9
ISSN: 0885-8985
Reference Cited: 0
CODEN: IESMEA
Inspec Accession Number: 4272928

Abstract:
The authors describe how the evolution of digital ASICs from first attempts to VLSI was accelerated in creating a 115000-gate equivalent array, in a 340-pin quad flat pack, within three generations. The first generation consisted of a 7800 gate eq. array containing the `glue logic' for a MIL-STD-1553B, dual redundant serial **bus**. CAE workstations were used to create the design, and vendor-specific tools were used for final simulations only. The second generation fully embedded the 1553 into the array, along the control **registers**, timers, counters, **interrupt** prioritorization and control, memory management, and DNA control circuitry to support an Intel 80960 CPU. The third

h eee e eee g e ch ch b c be be be c e eee

generation, a 115000 gate eq. array, added a second 1553, three UARTs, and two SDLC serial ports, permitting the creation of a stand-alone computer-I/O card in a single assembly. The third-generation ASIC was created from the second-generation netlist with the addition of vendor-supplied macro circuits, compiled circuits, and synthesized circuits. The utilization of a test vector generation language aided the design process

Index Terms:

VLSI application specific integrated circuits digital integrated circuits CAE workstations DNA control circuitry Intel 80960 CPU MIL-STD-1553B SDLC serial ports VLSI array compiled circuits digital ASICs dual redundant serial **bus** first generation ASIC glue logic **interrupt** prioritorization macro circuits memory management quad flat pack second generation ASIC second-generation netlist simulations synthesized circuits test vector generation language third-generation ASIC

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 216 KB] PREV NEXT DOWNLOAD CITATION

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

h eee e eee g e ch ch b c be be be c e eee

High speed data bus macro instruction set architecture

Prohofsky, T.
Unisys Corp., St. Paul, MN, USA;

This paper appears in: **Aerospace and Electronics Conference, 1991. NAECON 1991., Proceedings of the IEEE 1991 National**

Meeting Date: 05/20/1991 - 05/24/1991
Publication Date: 20-24 May 1991
Location: Dayton, OH USA
On page(s): 192 - 196 vol.1
Reference Cited: 4
Inspec Accession Number: 4143398

Abstract:
Unisys Corporation has developed an input/output (I/O) instruction set architecture (ISA) to accommodate I/O devices in reduced instruction set computing (RISC)-based applications. Control over the linear high speed data **bus** (HSDB) interface is implemented by control **registers**, memory resident instructions, and memory maps. Instruction chaining allows for autonomous multiple message transmission in addition to single message-by-message control. Handling data reception is customized by the mapping structure, which incorporates message polling, single and multiple message **interrupts**, and single and multiple message FIFOs. Control **registers** provide for

h eee e eee g e ch ch b c be be be c e eeec

transitioning between various modes and states within the I/O interface. By defining network accessible control **registers**, a method is made available for remote interface control. By combining remote interface control and message mapping, some applications may not require a processor to control each I/O interface

Index Terms:

computer interfaces instruction sets **interrupts** military computing reduced instruction set computing storage management FIFOs I/O interface RISC Unisys Corporation autonomous multiple message transmission control **registers** instruction chaining linear high speed data **bus** macro instruction set architecture memory maps memory resident instructions message **interrupts** message mapping message polling reduced instruction set computing remote interface control

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 328 KB] NEXT DOWNLOAD CITATION

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

h eee e eee g e ch ch b c be be be c e eeec

L5: Entry 3 of 46 File: USPT Jun 17, 2003

DOCUMENT-IDENTIFIER: US 6581119 B1
TITLE: Interrupt controller and a microcomputer incorporating this controller

Abstract Text (1):
To downsize the circuit scale of a CPU in a microcomputer capable of executing multiple interrupt, an interrupt controller includes an interrupt mask level register. The CPU temporarily transfers or stacks processing data into a RAM. The processing data include a PSR (i.e., system register) value and a PC (i.e., program counter) value of the interrupt processing presently running in CPU. At the same time, the CPU sends a stack signal "STK" to the interrupt controller. In response to the stack signal "STK", the interrupt controller temporarily transfers the interrupt mask level stored in the register into the RAM. When the CPU restarts the suspended interrupt processing, the CPU reads the PSR value and the PC value from the RAM while the CPU produces a return signal "RTN." In response to the return signal "RTN", the interrupt mask level is returned from the RAM to the register.

Detailed Description Text (8):
On the other hand, the interrupt controller 4 comprises an interrupt priority setting register 42, a priority judging circuit 44, an interrupt mask level register 46, and a comparator 48. The interrupt priority setting register 42 sets beforehand the priority to the interrupt processing corresponding to each interrupt request signal entered from the above-described peripheral circuits 10. The priority judging circuit 44 receives a plurality of priority values produced from the interrupt priority setting register 42 which correspond to a plurality of interrupt request signals simultaneously entered to the interrupt priority setting register 42. Then, the priority judging circuit 44 selects an interrupt request signal having a highest priority with reference to the received priority values. The interrupt mask level register 46 stores an interrupt mask level which represents the priority of the interrupt processing presently running in CPU 2. The comparator 48 compares the priority of the selected interrupt request signal, which is recognized by the priority judging circuit 44 as having the highest priority, with the interrupt mask level stored in the interrupt mask level register 46. When the priority of the interrupt request signal newly selected by the priority judging circuit 44 is higher than the priority of the interrupt processing presently running in CPU 2, the comparator 48 sends a CPU interrupt request signal "INTR" to CPU 2.

Detailed Description Text (20):
The processing of step 130 is performed for simultaneously transferring the above data into the predetermined stack area in RAM 6, namely, for the simultaneously stacking of the PSR value and the PC value of the interrupt processing suspended in response to the CPU interrupt request signal "INTR" as well as the interrupt mask level of this suspended interrupt processing. To this end, the data (i.e., PSR value and PC value) in the system register (PSR) 26 and the program counter (PC) 28 is sent via predetermined signal lines of the data bus 9 which are different from the signal lines for the interrupt mask level register 46. More specifically, among a plurality of signal lines corresponding to all bits (32 bits in this embodiment), three signal lines corresponding to the upper 3 bits are used for outputting the interrupt mask level. On the other hand, the signal lines used for outputting the PSR value and the PC value are different from the above three signal lines

dedicated to the interrupt mask level.

Detailed Description Text (21):
FIG. 3 shows a detailed allocation of the signal lines in the data bus 9. The signal lines for the upper 3 bits are used to transmit the interrupt mask level from the interrupt mask level register 46 to RAM 6. The signal lines for the lower 24 bits are used to transmit the data (i.e., PC value of 24 bits) of the program counter (PC) 28 to RAM 6. The signal lines for the remaining 5 bits are used to transmit the data (i.e., PSR value of 5 bits) of the system register (PSR) 26 to RAM 6.

Detailed Description Text (27):
Furthermore, according to the above-described embodiment, CPU 2 suspends the presently running interrupt processing when CPU 2 receives the CPU interrupt request signal "INTR" from the interrupt controller 4. When CPU 2 starts new interrupt processing while suspending the presently running interrupt processing, CPU 2 temporarily transfers the processing data (i.e., PSR value, PC value) of the suspended interrupt processing into the stack area of RAM 6. The processing data thus temporarily transferred into RAM 6 are required in restarting the suspended interrupt processing. At the same time, the interrupt mask level stored in the interrupt mask level register 46 is temporarily transferred into the predetermined stack area of RAM 6. When CPU 2 restarts the suspended interrupt processing, CPU 2 reads out the processing data (i.e., PSR value and PC value) from RAM 6. The readout processing data (i.e., PSR value and PC value) are written into the system register (PSR) 26 and the program counter (PC) 28, respectively. At the same time, the interrupt mask level register 46 reads out the interrupt mask level from RAM 6 and renews an interrupt mask level presently stored therein by the readout interrupt mask level.

Detailed Description Text (31):
Furthermore, in the above-described embodiment, the interrupt mask level is 3 bits. However, the kinds of interrupt request signals entered from the peripheral circuits 10 may be few. The priority of each interrupt request signal may be expressed by a binary data of 2 bits. In such a case, the interrupt mask level register 46 can be arranged to store a binary data of 2 bits. And, the interrupt mask level of two bits is transmitted from the interrupt controller 4 to RAM 6. On the other hand, the kinds of interrupt request signals entered from the peripheral circuits 10 may be many. The priority of each interrupt request signal may not be expressed by a binary data of 3 bits. In this case, the bit number of the interrupt mask level register 46 should be set to an appropriate value agreeable to the bit number (e.g., 5 bits) of the binary data representing the priority. Furthermore, it is preferable to divide the transmission of the interrupt mask level (5 bits) into two stages; a first stage is a transmission for the upper 3 bits and a second stage is a transmission for the lower 2 bits.

First Hit Fwd Refs

Generate Collection Print

L5: Entry 3 of 46 File: USPT Jun 17, 2003

US-PAT-NO: 6581119
DOCUMENT-IDENTIFIER: US 6581119 B1

TITLE: Interrupt controller and a microcomputer incorporating this controller

DATE-ISSUED: June 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Maeda; Kouichi	Anjo			JP
Ishihara; Hideaki	Okazaki			JP
Noda; Sinichi	Okazaki			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Denso Corporation	Kariya			JP	03

APPL-NO: 09/ 598321 [PALM]
DATE FILED: June 21, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-177064	June 23, 1999
JP	2000-152589	May 24, 2000

INT-CL: [07] G06 F 13/24, G06 F 13/26, G06 F 13/32

US-CL-ISSUED: 710/260; 710/261, 710/262, 710/263, 710/264, 710/265, 710/266, 710/267, 710/268, 710/269
US-CL-CURRENT: 710/260; 710/261, 710/262, 710/263, 710/264, 710/265, 710/266, 710/267, 710/268, 710/269

FIELD-OF-SEARCH: 710/260-269

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4001783	January 1977	Monahan et al.	710/264
☐	4734882	March 1988	Romagosa	710/264

h e b b g e e e f c e g c e ge

☐	5850558	December 1998	Qureshi et al.	
☐	5928348	July 1999	Mukai et al.	710/263
☐	5968159	October 1999	Mattheis	710/264

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0614148	September 1994	EP	
0886217	December 1998	EP	
2287806	September 1995	GB	
3-28951	February 1991	JP	
5-73472	March 1993	JP	
9-330236	March 1998	JP	
11-110233	April 1999	JP	

ART-UNIT: 2189

PRIMARY-EXAMINER: Auve; Glenn A.

ASSISTANT-EXAMINER: Vu; Trisha

ATTY-AGENT-FIRM: Posz & Bethards, PLC

ABSTRACT:

To downsize the circuit scale of a CPU in a microcomputer capable of executing multiple interrupt, an interrupt controller includes an interrupt mask level register. The CPU temporarily transfers or stacks processing data into a RAM. The processing data include a PSR (i.e., system register) value and a PC (i.e., program counter) value of the interrupt processing presently running in CPU. At the same time, the CPU sends a stack signal "STK" to the interrupt controller. In response to the stack signal "STK", the interrupt controller temporarily transfers the interrupt mask level stored in the register into the RAM. When the CPU restarts the suspended interrupt processing, the CPU reads the PSR value and the PC value from the RAM while the CPU produces a return signal "RTN." In response to the return signal "RTN", the interrupt mask level is returned from the RAM to the register.

3 Claims, 4 Drawing figures

h e b b g e e e f c e g c e ge

First Hit Fwd Refs

Generate Collection Print

L7: Entry 12 of 39 File: USPT Dec 8, 1998

DOCUMENT-IDENTIFIER: US 5848237 A
TITLE: Programmable digital filter for stable interval detection

CLAIMS:

16. The peripheral device of claim 15 further comprising:

an interrupt mask register which is coupled to receive an interrupt mask value from said bus and which is coupled to said state machine to selectably prevent said peripheral device from interrupting said processor according to said interrupt mask value.

h e b b cg b cc e

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L2: Entry 77 of 77 File: USPT Jul 11, 1972

DOCUMENT-IDENTIFIER: US 3676861 A
TITLE: MULTIPLE MASK REGISTERS FOR SERVICING INTERRUPTS IN A MULTIPROCESSOR SYSTEM

Brief Summary Text (8):
A mask register is provided in a system controller that stores the priority rating of the program being processed by a control module. Another register stores the interrupt requests for processing time or access to a module in the system. The mask register selectively prevents the interrupt from being serviced by the control module associated with the mask register by disabling a priority select interrupt logic circuitry that prevents the transmission of the interrupt signals to the control module. At the completion of the program by the control module the control module requests the highest priority interrupt signal stored in the interrupt register. The interrupt signals are sent to the interrupt registers by the modules requesting an interrupt. A priority rating signal set as well as an identification signal are included with the interrupt signal. This priority rating signal places the interrupt signal in a priority tree logic circuitry. The priority tree permits the servicing of interrupts at the highest level first by any of the control modules, thus providing for the servicing of the interrupts by several processors set as control processors rather than having only one processor servicing interrupts.

First Hit Fwd Refs

Generate Collection Print

L2: Entry 43 of 77 File: USPT Mar 17, 1998

DOCUMENT-IDENTIFIER: US 5729720 A
TITLE: Power management masked clock circuitry, systems and methods

Detailed Description Text (812):
In FIG. 44, the Interrupt Request register stores requests from all channels requesting service. Its bits are labeled using channel names IR7-0. Corresponding to the channel names, the in-service register bits are named IS7-0. These bits indicate which channels are currently being serviced. The Interrupt Mask register permits the CPU to disable any or all interrupt channels. The priority resolver evaluates inputs from the above three registers, issues interrupts, and latches the corresponding bits into the in-service G54 register. A master controller of FIG. 43 outputs a code to the slave device during interrupt acknowledge cycles. This output is compared in the cascade buffer/comparator with a 3-bit identification code (previously written). If the codes match, the slave controller generates an interrupt vector. The contents of the Vector register provide the CPU with the appropriate interrupt vector.

First Hit Fwd Refs

Generate Collection Print

L2: Entry 43 of 77 File: USPT Mar 17, 1998

US-PAT-NO: 5729720
DOCUMENT-IDENTIFIER: US 5729720 A

TITLE: Power management masked clock circuitry, systems and methods

DATE-ISSUED: March 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kau; Weiyuen	Dallas	TX		
Walsh; James J.	Plano	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 759396 [PALM]
DATE FILED: December 4, 1996

PARENT-CASE:
This application is a continuation of application Ser. No. 08/486,423, now abandoned, which is a continuation of application Ser. No. 08/362,669 filed Dec. 22, 1994, now abandoned.

INT-CL: [06] G06 F 1/04

US-CL-ISSUED: 395/555; 395/556
US-CL-CURRENT: 713/500; 713/501

FIELD-OF-SEARCH: 395/555, 395/556, 395/559, 395/560, 395/750.04, 327/175

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3678463	July 1972	Peters	340/172.5
☐	4590553	May 1986	Noda	364/200
☐	4835728	May 1989	Si et al.	364/900
☐	4916697	April 1990	Roche et al.	371/14

h e b b g e e e f c e e ge

☐	5025387	June 1991	Frane	364/493
☐	5175853	December 1992	Kardach et al.	395/650
☐	5189647	February 1993	Suzuki et al.	368/10
☐	5254888	October 1993	Lee et al.	307/480
☐	5276888	January 1994	Kardach et al.	395/725
☐	5287292	February 1994	Kenny et al.	364/550
☐	5313108	May 1994	Lee et al.	307/267
☐	5388265	February 1995	Volk	395/750
☐	5390350	February 1995	Chung et al.	395/150
☐	5451892	September 1995	Bailey	327/113
☐	5452434	September 1995	MacDonald	395/550
☐	5465367	November 1995	Reddy et al.	395/750
☐	5471635	November 1995	Williams	395/800
☐	5473767	December 1995	Kardach et al.	395/550
☐	5485127	January 1996	Bertoluzzi et al.	331/69
☐	5537581	July 1996	Conary et al.	395/550

OTHER PUBLICATIONS

Linley Gwennap, Microprocessor Report, "TI Shows Integrated X86 CPU for Notebooks",vol. 8, No.2. Feb. 14, 1994, pp. 5-7.
ACC Micro, 2056 3.3V Pentium Single Chip Solution for Notebook Applications, Rev. 1.1, pp. 1-1 -1-10.
ACC Micro, 2066 486/386DX Notebook Enhanced-SL Single Chip AT, Rev. 1.2, Oct. 11, 1993 pp.1-1 -1-10.
PicoPower Redwood, Technical Reference Manual,Databook 3.0P, Jul. 8, 1994, pp.i-iv, 1-23, 25, 56-87, 94-97.
PicoPower "Evergreen" 486/386DX Portable Computer Core Chip, Version 1.3.1, Sep. 16, 92, pp. i -iv, 21-31, 35 -39, 53 -71.
Intel486 SL Microprocessor SuperSet System Design Guide, System and Power Management, Chapter 12, 1992, pp. 12-1 -12-38.
Intel386 SL Microprocessor SuperSet System Design Guide, System and Power Management, Chapter 14, 1992, pp. 14-1 -14-28.
Intel386 SL Microprocessor SuperSet Programmer's Reference Manual, System and Power Management, Chapter 6, 1992, pp. 6-1 -6-56.
OPTi Single Chip Notebook SCNB, Data Book Version 2.0 Mar. 18, 93, pp. 1-2, 8-20.
82C836 ChipSet, Single-Chip 386SX AT Data Book, Dec. 1990. pp. 1-6, 9 -11.
Intel386 SL Microprocessor SuperSet System Design Guide, 386 SL CPU to 82360 SL Interface, 1992, Chapter 3, pp. 3-1 -3-11.
Intel486 SL Microprocessor SuperSet System Design Guide, 486 SL CPU to 82360 SL Interface, 1992 Chapter 3, pp. 3-1 -3-12.
Intel386 SL Microprocessor SuperSet System Design Guide, The SL SuperSet System Design Guide, The SL SuperSet Extension Registers, Chapter 10, pp. 10-1, 10-2, 10-12, 10-127 -10-149, 10-172 -10-183, 10-188 -10-190.
OPTi Python Chipset for Pentium Processors, 82C546 & 82C547 Data Book Version 1.0, May 1994, pp. 61, 72.
Tidalwave, TM8100A, Advanced 486SLC/SXLC Palmtop Single Chip, Rev. 1.6, pp. 1-5, 12-15, 36-38, 42-46, pp. 1, 4, 5.
Vadem, VG-230 Sub-Notebook Engine Data Manual, Nov. 1992, pp.1-5,17-29, 76-83, 95-97.

Western Digital WD8110/LV System Controller 80486SX/DX PC/AT Compatible Desktop, Laptop, Palmtop, and Pen-Based Computers, Sep. 15, 1993, pp. 1-5, 7-9, 30-40, 93-126.
Symphony Laboratories, Wagner 486 PC/AT Chip Set, Rev A.2,Feature, Block Diagram, pp. 1-9 -1-14.
ALI, M1709 High Performance VESA/PCI/ISA Notebook Chipset, Product Brief, Jan. 8, 1994.
UMC Super Energy Star Green File, Version 4.0, Preliminary UM8881F/8886F Apr. 15, 1994, pp. 15-18, 37-42.
UMC Super Energy Star Green File, Version 4.0, Preliminary UM8486F Apr. 15, 1994, pp. 6-8, 15-17, 21-30.
UMC Super Energy Star Green File, Version 4.0, Preliminary UM8498F/8496F/82C495F Apr. 15, 1994, pp. 1-3, 25-32, 1.
OPTi, Viper Notebook Chipset, 82C556/82C557/82C558N, pp. 1-5, 90 -116.
Texas Instruments, TACT83000 AT Chip Set, PC Systems Logic, 1991. pp. 2-51 -2-54.
OPTi 82C802G, System/Power Management Controller, Mar. 1994, pp. 1-18, 26, 34 -44.
OPTi 82C596/82C597, Cobra Chipset for Pentium Processors, Data Book Rev. 1.0, Oct. 1994, pp.1-3,60.
KOALA, Power Management Master, Rev. 0.1 May 1992, pp.2-26,???.
Texas Instruments, Tiffany Single-Chip System Logic for 386SX/486SLC-Based Palmtop / Sub-notebook PCs, User's Guide Preliminary Rev. 1.4, May 1993, pp. 1-5, 12, 13, 36, 37, 45, 46.
PicoPower "Evergreen HV" PT86C268, Version 1.0.2, Mar. 9, 1993, pp. i-iii,20-28, 58-76, 38-44.
EFAR, EC802G, One Chip 32 Bits PC/AT Core Logic, Technical Reference Manual, 1994, pp. 11-13, 32 -45, 64-80, 93, 96.
Texas Instruments, TACT84411 Single-Chip 80486, Systems Logic, 1993. pp. 1-1 -1-5, 2-1, 2-2, 5-9, 5-10.

ART-UNIT: 236

PRIMARY-EXAMINER: Butler; Dennis M.

ATTY-AGENT-FIRM: Burton; Dana L. Kesterson; James C. Donaldson; Richard L.

ABSTRACT:

An electronic system (100) includes a register (TONTOFF) for data and a clock circuit (2340, 708) coupled to the register and responsive to the data in the register to generate a series of clock pulses (CPU.sub.-- CLK). The series of clock pulses occupies time intervals (2550) interspersed with time intervals free of clock pulses (2552), as an output having a ratio of the time intervals responsive to the data. Other devices, systems and methods are also disclosed.

43 Claims, 112 Drawing figures

L2: Entry 15 of 77 File: USPT Feb 15, 2000

DOCUMENT-IDENTIFIER: US 6025855 A
**** See image for Certificate of Correction ****
TITLE: Store double word and status word write graphics primitives

Detailed Description Text (22):
The other registers in the graphics device of significance are a hardware status mask register 319 and a hardware status vector address register 318, both in the internal operating registers 316 of the command stream controller 204. The hardware status mask register 319 enables or disables masking of a signal from the interrupt status register 317 in response to a status bit change. A store double word is only reported to the cacheable memory 116 if the signal is not masked. The hardware vector address register 318 contains the cacheable address where the contents of the interrupt status register 317 are reported. As previously mentioned, any change in any of the bits in the interrupt status register 317 results in the status being reported to the cacheable memory 116 if the corresponding bit is not masked off in the hardware status mask register 319.

First Hit Fwd Refs

Generate Collection Print

L2: Entry 15 of 77 File: USPT Feb 15, 2000

US-PAT-NO: 6025855
DOCUMENT-IDENTIFIER: US 6025855 A
** See image for Certificate of Correction **

TITLE: Store double word and status word write graphics primitives

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Meinerth; Kim A.	Granite Bay	CA		
Sreenivas; Aditya	El Dorado Hills	CA		
Sreenivas; Krishnan	Rancho Cordova	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 09/ 021231 [PALM]
DATE FILED: February 10, 1998

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 345/514; 345/513, 345/522, 345/515
US-CL-CURRENT: 345/556; 345/522, 345/557

FIELD-OF-SEARCH: 345/501, 345/507, 345/509, 345/513-516, 345/522, 395/681, 395/682

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4598384	July 1986	Shaw et al.	345/116
☐	5440746	August 1995	Lentz	345/504
☐	5481276	January 1996	Dickey et al.	345/132
☐	5745761	April 1998	Celi, Jr. et al.	395/681

h e b b g e e e f c e e ge

ART-UNIT: 276

PRIMARY-EXAMINER: Tung; Kee M.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

A method for communicating graphics device status information to a graphics driver. Status of a graphics device is checked to determine whether the graphics device is ready to process a next instruction. A location in cacheable memory accessible to a graphics driver is updated with the status. The graphics driver reads the status to determine when to generate the next instruction for processing by the graphics data. A first instruction to be forwarded to the graphics device is generated. A status in an operating register in the graphics device is updated indicating that an event is being monitored. The updating is performed in response to receipt of the first instruction by the graphics device. The status is written to a second cacheable location in system memory accessible to the graphics driver. A second instruction is generated by the graphics driver to provide a predetermined address and instruction completion data to the graphics device.

12 Claims, 7 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L2: Entry 2 of 77 File: USPT Jan 20, 2004

DOCUMENT-IDENTIFIER: US 6681261 B2
TITLE: Programmable matrix switch

Detailed Description Text (88):
Both positive and negative edge interrupt registers 406 and 408 have corresponding mask (or enable) registers 410 and 412, respectively. Mask registers 410 and 412 are used to mask and unmask the edge interrupt bits in the corresponding edge interrupt registers. A zero in the mask register masks (disables) the corresponding bit in the associated edge interrupt register; a one in the mask register unmasks (enables) the corresponding bit in the associated edge interrupt register. When an edge interrupt bit is masked, it cannot generate an interrupt signal; whereas when it is unmasked, it can. An OR gate 414 ORs all of the unmasked negative edge interrupt bits together to produce a Phantom negative signal 416 that controls the state of the Low Priority Interrupt Bit in the port module cards status and control register. Similarly, an OR gate 418 ORs all of the unmasked positive edge interrupt bits together to produce a Phantom positive signal 420 that controls the state of the High Priority Interrupt Bit in the port module cards status and control register. Finally, an OR gate 422 ORs all of the unmasked positive and negative edge interrupt bits together to produce a Summary Port Module Interrupt signal 424 that is sent over the backplane to the controller module. In other words, any bit set in any edge register causes the summary port module interrupt signal to be on (provided that interrupt bit has not been disabled). The summary interrupt signal stays on until all of the set edge interrupt register bits are cleared or disabled and enabling a set bit causes the summary interrupt signal to go on.

h e b b cg b cc e

First Hit Fwd Refs

Generate Collection Print

L2: Entry 2 of 77 File: USPT Jan 20, 2004

US-PAT-NO: 6681261
DOCUMENT-IDENTIFIER: US 6681261 B2

TITLE: Programmable matrix switch

DATE-ISSUED: January 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mancusi; Michael D.	Holliston	MA		
Massery; Joseph E.	Westborough	MA		
Osmond; Roger F.	Littleton	MA		
Fitzgerald; Michael J.	Framingham	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Storage Technology Corporation	Louisville	CO			02

APPL-NO: 10/ 061929 [PALM]
DATE FILED: February 1, 2002

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This is a continuation of U.S. patent application Ser. No. 09/632,284, filed Aug. 8, 2000, now U.S. Pat. No. 6,418,481, which is a continuation of U.S. patent application Ser. No. 08/294,882, filed Aug. 23, 1994, now U.S. Pat. No. 6,275,864, which is a continuation of U.S. patent application Ser. No. 07/829,119, filed Jan. 31, 1992, now abandoned which is a continuation-in-part of U.S. patent application Ser. No. 07/744,295 entitled "Network Management System for a Freely Configurable Network", filed on Aug. 13, 1991, now abandoned.

INT-CL: [07] G06 F 15/16

US-CL-ISSUED: 709/250; 709/220, 709/249
US-CL-CURRENT: 709/250; 709/220, 709/249

FIELD-OF-SEARCH: 709/250, 709/251, 709/227, 709/223, 709/220, 709/249

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

h e b b g e e e f c e e ge

☐	4032893	June 1977	Moran	
☐	4255741	March 1981	Peterson	
☐	4393497	July 1983	Cantwell, Jr.	
☐	4633245	December 1986	Blount et al.	
☐	4674085	June 1987	Aranguren et al.	
☐	4772811	September 1988	Fujioka et al.	
☐	4845706	July 1989	Franaszek	
☐	4872197	October 1989	Pemmaraju	
☐	4899333	February 1990	Roediger	
☐	4933936	June 1990	Rasmussen et al.	
☐	5048014	September 1991	Fischer	
☐	5138615	August 1992	Lamport et al.	
☐	5140585	August 1992	Tomikawa	
☐	5214646	May 1993	Yacoby	
☐	5224108	June 1993	McDysan et al.	
☐	5226039	July 1993	Frank et al.	
☐	5274637	December 1993	Sakamura et al.	
☐	5301303	April 1994	Abraham et al.	
☐	5343516	August 1994	Callele et al.	379/93.05
☐	6275864	August 2001	Mancusi et al.	709/250
☐	6470007	October 2002	Berman	370/351

ART-UNIT: 2154

PRIMARY-EXAMINER: Maung; Zarni

ATTY-AGENT-FIRM: Brooks Kushman P.C.

ABSTRACT:

A system and method for interconnecting a plurality of network components to form a local area network (LAN) include a wiring manager having at least one port module connected to a controller via a data signal bus on a passive backplane. Each port module includes a plurality of ports which can be programmed to electrically couple selected sets of the plurality of network components without physically rerouting network cabling. A LAN management system provides a graphical user interface to communicate with the wiring manager and provide network status information and control the wiring manager to configure the network.

14 Claims, 17 Drawing figures

h e b b g e e e f c e e ge

US-PAT-NO: H001385

DOCUMENT-IDENTIFIER: US H001385 H

TITLE: High speed computer application specific integrated circuit

---------- KWIC ---------

Detailed Description Text - DETX (117):

One or more interrupts can be disabled as directed by the software. All 23 external interrupts can be masked by writing a 12-bit value to the two mask registers. To enable a certain interrupt, the programmer must write a "1" to the corresponding bit in one of the two mask registers. The MSB of one of the mask registers will totally disable all 23 interrupt inputs if it is set to a "1". If it is set to a "0", the 23 interrupt inputs will be enabled or disabled according to the way the remaining bits in the mask registers are set. This MSB is known as the global enable bit. The second MSB of one of the mask registers enables or disables the highest priority interrupt. The LSB of the other mask register enables or disables the lowest priority interrupt input. The remaining interrupt inputs are enabled or disabled by the remaining mask register bits, with descending interrupt priority. The polarity of the individual interrupt-enable bits is opposite to the polarity of the global interrupt-inhibit bit. If an interrupt control bit is a "1", the corresponding interrupt will be enabled. If an interrupt control bit is a "0", the corresponding interrupt will be disabled.

US000001385H

United States Statutory Invention Registration [19]

[11] Reg. Number: H1385

[43] Published: Dec. 6, 1994

Stickel et al.

[54] HIGH SPEED COMPUTER APPLICATION SPECIFIC INTEGRATED CIRCUIT

[75] Inventors: Karl D. Stickel; Sam T. Tsay; Michael J. Gibbault, all of Ridgecrest, Calif.

[73] Assignee: The United States of America as represented by the Secretary of the Navy, Washington, D.C.

[21] Appl. No.: 779,426

[22] Filed: Oct. 18, 1991

[51] Int. Cl.[5] G06F 7/00

[52] U.S. Cl. 395/800; 395/375

[58] Field of Search 395/375, 800

[56] References Cited

U.S. PATENT DOCUMENTS

4,794,521	12/1988	Ziegler et al.	395/425
4,984,151	1/1991	Dujari	395/775
4,989,113	1/1991	Hall, Jr. et al.	395/425
5,265,005	11/1993	Schmidt et al.	364/147

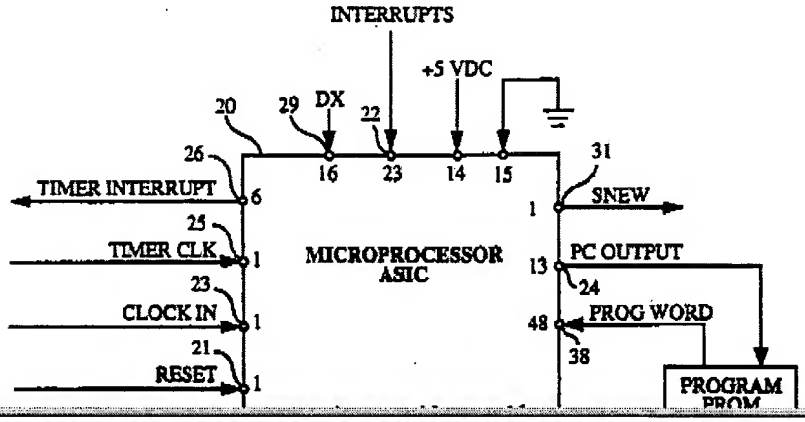
Primary Examiner—Bernarr E. Gregory

Attorney, Agent, or Firm—John L. Forrest, Jr.; Melvin J. Sliwka; Harvey A. Gilbert

[57] ABSTRACT

An integrated circuit chip for application in a computer for performing high speed arithmetic operations in hardware has hardware for forming a system clock processor circuit, a timer circuit, a program counter and branching circuit; an interrupt processor circuit formed in the chip; an interrupt address random access memory, mathematical computation circuitry and an internal data random access memory. The mathematical computation circuitry includes a circuit for performing combined division and square root operations. The integrated circuit operates on a fixed instruction set and provides the means for performing instruction and operand look-ahead to permit execution of each instruction in a single clock cycle.

6 Claims, 7 Drawing Sheets



US-PAT-NO: 4573118

DOCUMENT-IDENTIFIER: US 4573118 A

TITLE: Microprocessor with branch control

---------- KWIC ---------

Detailed Description Text - DETX (81):
There are 16 levels of interrupt prioritized on chip as indicated in Table 4. Nine are external, of which two are level sensitive (IOL.sub.1 INT, IOL.sub.2 INT). The other seven external interrupts are either level or edge-sensitive, according to the interrupt mode bit in the configuration register. All interrupts are latched into the pending interrupt register (PIR) 250 and may be disabled, or masked by the mask register (MK) 270, except as indicated in the table.

United States Patent [19]
Damouny et al.

[11] **Patent Number: 4,573,118**
[45] **Date of Patent: Feb. 25, 1986**

[54] **MICROPROCESSOR WITH BRANCH CONTROL**

[75] Inventors: **Nabil G. Damouny**, Sunnyvale; **Min-Shu Huang**, Mountain View, both of Calif.

[73] Assignee: **Fairchild Camera & Instrument Corporation**, Mountain View, Calif.

[21] Appl. No.: **481,061**

[22] Filed: **Mar. 31, 1983**

[51] Int. Cl.⁴ G06F 9/00
[52] U.S. Cl. 364/200
[58] Field of Search ..... 364/200 MS File

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,943,495 3/1976 Garlic 364/200

Primary Examiner—Raulfe B. Zache
Attorney, Agent, or Firm—Clifton L. Anderson; Carl L. Silverman; Dave Carroll

[57] **ABSTRACT**

A microprocessor data processing system (1700) includes system units (50, 1704) connected to a bus (1702), with a bus arbiter (1712) and a protocol for assigning bus access to the system units (50, 1704). The microprocessor (50) executes both arithmetic operations and floating point operations. A microcontrol store (162) stores common instructions usable in different floating point operations. A PLA (180) supplies addresses to microcontrol store (162) and provides a signal indicating floating point instruction type. The microprocessor (50) includes a pending interrupt register (250) connected to mask and enable logic (268). The mask and enable logic (268) is connected to a priority encoder (278), which is connected to an interrupt latch (282). The latch (282) supplies outputs to generate a current state storage address. Branch control logic (1938) receives branch conditions inputs and branch control information and generates control signals for a next micro address multiplexer (1934) in a pipelined instruction path.

10 Claims, 25 Drawing Figures